REMARKS

The Examiner rejected claims 1-6 under 35 U.S.C. § 102(b) as allegedly being anticipated by Lee (US Pat. 4,862,232).

Applicants respectfully traverse the § 102(b) rejections with the following arguments.

35 U.S.C. § 102(b)

The Examiner rejected claims 1-6 under 35 U.S.C. § 102(b) as allegedly being anticipated by Lee (US Pat. 4,862,232).

Regarding claim 1, Applicants respectfully contend that Lee does not anticipate claim 1, because Lee does not teach each and every feature of claim 1. For example, Lee does not teach "**a semiconductor layer**;... **a semiconductor buried well region**... wherein said dopants of the second doping polarity of the semiconductor buried well region have **a doping concentration higher** than that of the semiconductor layer" of claim 1 (bold emphasis added).

More specifically, FIG. 1 of Lee teaches a Si substrate 10. On one hand, if the Si substrate 10 is used to teach the "semiconductor buried well region" of claim 1 (as argued by the Examiner in bullet #2 of the Office Action), then Lee fails to teach the "semiconductor layer" of claim 1. On the other hand, if the Si substrate 10 is used to teach the "semiconductor layer" of claim 1, then Lee fails to teach the "semiconductor buried well region" of claim 1.

It should be noted that the "semiconductor layer" of claim 1 is supported in the specification by the semiconductor layer 110 (see FIG. 1I, paragraph 15, lines 1-3). The "semiconductor buried well region" of claim 1 is supported in the specification by the buried well region 130 (see FIG. 1I, paragraph 21, lines 1-3). The feature "said dopants of the second doping polarity of the semiconductor buried well region have a doping concentration higher than that of the semiconductor layer" of claim 1 is also supported in the specification (see paragraph 21, lines 1-3).

Based on the preceding arguments, Applicants respectfully maintain that Lee does not anticipate claim 1, and that claim 1 is in condition for allowance.

Regarding claims 4-6, since claims 4-6 depend from claim 1, Applicants contend that claims 4-6 are likewise in condition for allowance.

Moreover, regarding claim 4, Lee does not teach "wherein the semiconductor channel region and the gate dielectric layer are in direct physical contact with each other via a common interfacing surface that defines **a plane**, and wherein said defined plane **divides** the first source/drain region into two regions" of claim 4 (bold emphasis added). More specifically, in FIG. 1 of Lee, the plane defined by the common interfacing surface between the semiconductor channel region 30 and the gate dielectric layer 34 **does not divide** the first S/D region 14 into two regions as claimed in claim 4.

It should be noted that the limitation "wherein said defined plane divides the first source/drain region into two regions" of claim 4 is supported in the specification. More specifically, in FIG. 1I, the plane defined by the common interfacing surface between the semiconductor channel region 132 and the gate dielectric layer 135 **divides** the first S/D region 150a into two regions (see also paragraph 24, lines 1-4).

Moreover, regarding claim 5, Lee does not teach "wherein said defined plane **divides** the second source/drain region into two regions" of claim 5 (bold emphasis added). More specifically, in FIG. 1 of Lee, the plane defined by the common interfacing surface between the semiconductor channel region 30 and the gate dielectric layer 34 **does not divide** the second S/D region 16 into two regions as claimed in claim 5.

It should be noted that the limitation "wherein said defined plane divides the second source/drain region into two regions" of claim 5 is supported in the specification. More specifically, in FIG. 1I, the plane defined by the common interfacing surface between the

semiconductor channel region 132 and the gate dielectric layer 135 divides the second S/D region 150b into two regions (see also paragraph 24, lines 1-4).

Regarding claims 2 and 3, since claims 2 and 3 depend from claim 1, Applicants contend that claims 2 and 3 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

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